State Elements

State elements provide a means of storing values and controlling data flow in a circuit. The most basic state element is a D-type Flip-Flop (figure 1a). D and Q are single bit input and output, respectively. When n D flip-flops are connected in parallel and controlled by the same clock, they form an n-bit register. To determine the input and output values of state elements, timing diagrams are often used in digital circuit analysis.

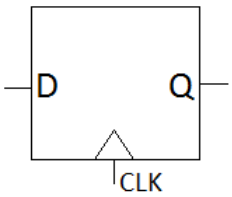
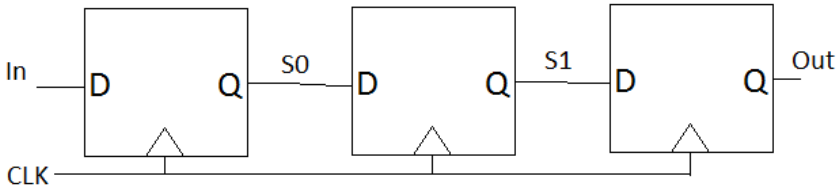


Figure 1a. D-type Flip-Flop



1b. Configuration for Q1.

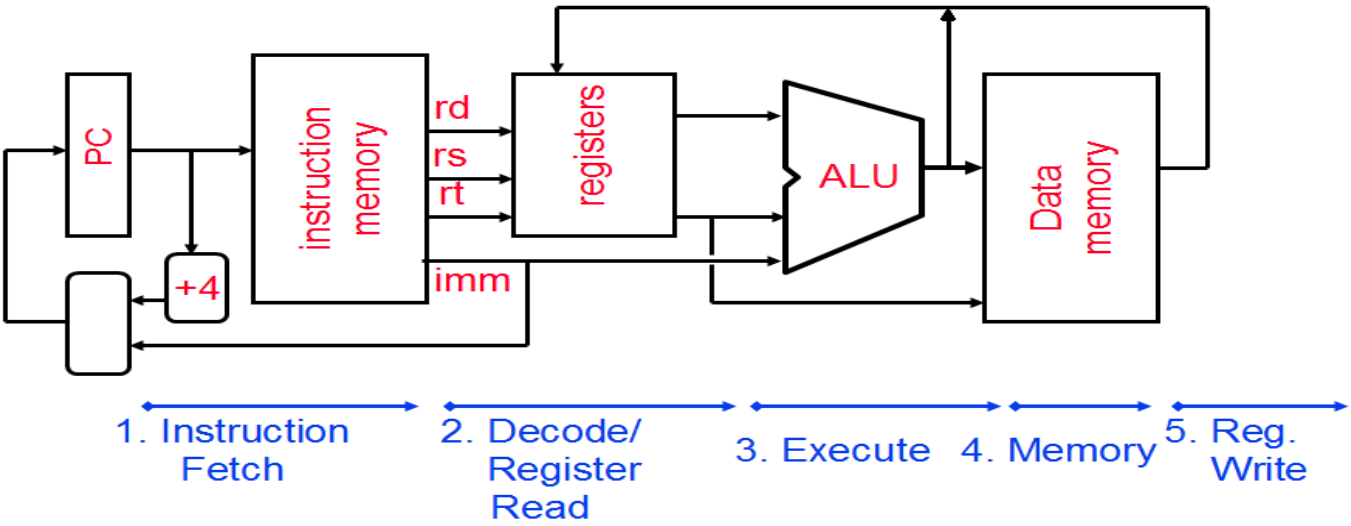
Q1: Figure 1b represents three D-type flip-flips connected in series. On the **rising edge** of the clock, the value from D is copied to Q, after a small delay (known as the Clk-to-Q delay). Complete the following timing diagrams for this configuration.

Register Transfer Language

RTL is used to describe flow of data. In MIPS, we use R[x] to represent the value of register x, and Mem[y] for the value at memory location y (similar to array syntax).

Single Cycle CPU

Below is the simplified datapath for a single cycle CPU as shown in class.



Q2: Label any unlabeled wires in the above diagram (use RTL if necessary).

Q3: We would like to modify our datapath to execute: add, ori, sw, bne, j.

Draw the new datapath, with necessary muxes and control signals. Then fill in the control table.

Assume ALU has an "=" output that is high when the two inputs are equal and low otherwise.

Instrs.	Control Signals							
add								
ori								
sw								
bne								
j								